GF22: 3.3V 32kHz Oscillators

Libraries

Name	Process	Form Factor
RGO_GF22_18V33_FDX_25C_OSC_032	FDX	Staggered CUP
RGO_GF22_18V33_FDX_45C_OSC_032	FDX	Inline CUP

Summary

The 3.3V 32kHz Oscillators library provides a 32kHz real time clock oscillator macro I/O cell. An adapter cell is included to utilize this oscillator with libraries based on the 1.8V pad ring bus structure.

These 22nm libraries are available in inline and staggered CUP wire bond implementations with a flip chip option.

To utilize these cells in the pad ring, an additional library is required – 3.3V Support: Power. That library contains the DVDD/DVSS power cells necessary for ESD protection, the POC and VREF cells, and a rail splitter to isolate the oscillator in its own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.
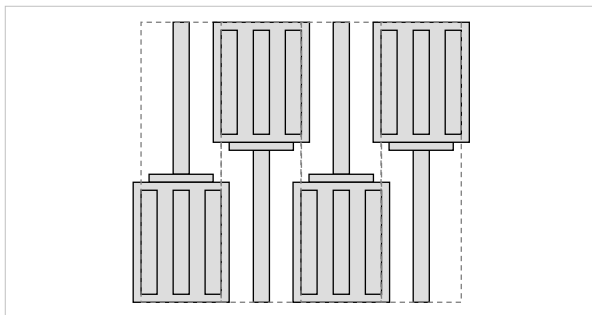
ESD Protection:
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)
    - 750V corner pin C4B package classification achieved by following key design priorities
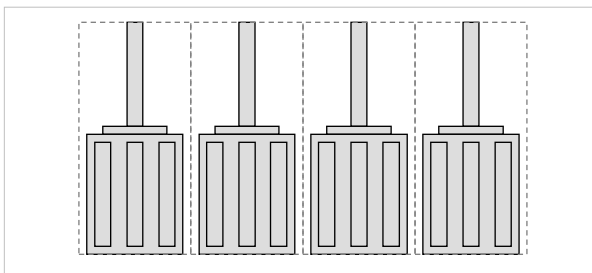
Latch-up Immunity:
- JEDEC compliant
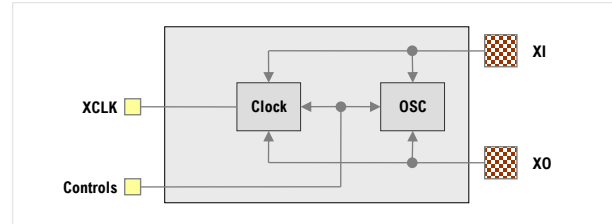 - Tested to I-Test criteria of ± 100mA @ 125°C

OSx_BI_032_1833V

32 KHz RTC Oscillator Features

- Designed to use a 32.786 kHz external crystal for Real Time Clock applications.
- Optimized for low power, stability and minimum jitter
- Characterized with crystal loading capacitors ranging from 8 pF to 35 pF.
- Speed-up circuitry for fast startup
- Power-down mode]
- Bypass mode
- Operates on core power only (VDD/VSS cells embedded)

Vertical-only (_V) and and horizontal-only (_H) variants provided.

Cell Size & Form Factor

Staggered (pad-limited) – 120µm x 165µm

Inline (core-limited) – 216µm x 95µm

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.9	0.945	V
		0.72	0.8	0.88	V
		0.59	0.65	0.715	V
		0.45	0.5	0.55	V
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
		1.35	1.5	1.65	V
		1.08	1.2	1.32	V
T_J	Junction temperature	-40	25	150	°C
V_{PAD}	Voltage at XI / XO [1]	0	-	V_{VDD}	V

[1] XI can be driven by an external clock for bypass operation. XO should never be driven or loaded by anything other than the oscillator crystal.

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
0.65V (AG2)	FFG	+10%	+10%	-40°C
	FFG	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	0.59V	-10%	-40°C
	SSG	0.59V	-10%	125°C
0.8V / 0.5V (AG2)	FFG	+10%	+10%	-40°C
	FFG	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	-10%	-10%	-40°C
	SSG	-10%	-10%	125°C
0.9V Overdrive (AG2)	FFG	+5%	+10%	-40°C
	FFG	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	-10%	-10%	-40°C
	SSG	-10%	-10%	125°C
0.8V (AG1)	FFG	+5%	+10%	-40°C
	FFG	+5%	+10%	125°C
	FFG	+5%	+10%	150°C
	SSG	-10%	-10%	150°C

[1] DVDD = 1.2V, 1.5V, 1.8V, 2.5V & 3.3V